

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1-2. (canceled)

Claim 3. (currently amended): A semiconductor device comprising:

an insulating underlayer;

a first insulating interlayer formed on said insulating underlayer, said first insulating interlayer having a groove;

a first metal layer having silicon atoms diffused within said first metal layer, and wherein said first metal layer is buried in said groove; and

a first metal diffusion barrier layer formed on said first metal layer and said first insulating interlayer, wherein

said first insulating interlayer comprises at least one layer selected from the group consisting of a SiO₂ layer, and a low-k material layer; and

~~wherein said low-k material layer comprises one of a SiOF layer, a SiOC layer, a ladder-type hydrogen siloxane layer and a porous ladder-type hydrogen siloxane layer.~~

Claim 4. (original): The device as set forth in claim 3, wherein said ladder-type hydrogen siloxane layer comprises an L-OxTM layer.

Claim 5. (original): The device as set forth in claim 3, wherein said ladder-type hydrogen siloxane layer has a density of about 1.50 g/cm^3 to 1.58 g/cm^3 .

Claim 6. (original): The device as set forth in claim 3, wherein said ladder-type hydrogen siloxane layer has a refractive index of about 1.38 to 1.40 at a wavelength of about 633 nm.

Claim 7. (original): The device as set forth in claim 3, further comprising a mask insulating layer made of silicon dioxide formed on the one of said ladder-type hydrogen siloxane layer and said porous ladder-type hydrogen siloxane layer.

Claims 8-14. (canceled).

Claim 15. (previously presented): A semiconductor device comprising:

an insulating underlayer;

a first insulating interlayer formed on said insulating underlayer, said first insulating interlayer having a groove;

a first metal layer having silicon atoms diffused within said first metal layer, and wherein said first metal layer is buried in said groove; and

a first metal diffusion barrier layer formed on said first metal layer and said first insulating interlayer, wherein said first metal diffusion barrier layer comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

Claim 16. (previously presented): A semiconductor device comprising:

an insulating underlayer;

a first insulating interlayer formed on said insulating underlayer, said first insulating interlayer having a groove;

a first metal layer having silicon atoms diffused within said first metal layer, and wherein said first metal layer is buried in said groove;

a first metal diffusion barrier layer formed on said first silicon-diffused metal layer and said first insulating interlayer; and

a first etching stopper between said insulating underlayer and said first insulating interlayer.

Claim 17. (previously presented): The device as set forth in claim 16, wherein said first etching stopper is a SiCN layer.

Claims 18-50. (canceled).

Claim 51. (previously presented): A semiconductor device comprising:

an insulating underlayer;

an insulating interlayer formed on said insulating underlayer, said insulating interlayer having a groove;

a barrier metal layer made of at least one of Ta, TaN, Ti, TiN, TaSiN and TiSiN formed within said groove;

a silicon-diffused copper layer including no copper silicide formed thereon and buried in said groove on said barrier metal layer, said silicon-diffused copper layer having a silicon component of less than 8 atoms %; and

a copper diffusion barrier layer made of at least one of SiCN, SiC, SiOC and organic material and formed on said silicon-diffused copper layer and said insulating interlayer.

Claims 52-214. (canceled).

Claim 215. (previously presented): A semiconductor device comprising:

an insulating underlayer;

a first insulating interlayer formed on said insulating underlayer, said first insulating interlayer having a groove;

a first metal layer having silicon atoms diffused within said first metal layer, and wherein said first metal layer is buried in said groove; and

a first metal diffusion barrier layer formed on said first metal layer and said first insulating interlayer,

wherein said first silicon-diffused metal layer has a larger silicon concentration near an upper side thereof than near a lower side thereof.

Claim 216. (previously presented): A semiconductor device comprising:

an insulating underlayer;

a first insulating interlayer formed on said insulating underlayer, said first insulating interlayer having a groove;

a first metal layer having silicon atoms diffused within said first metal layer, and wherein said metal layer is buried in said groove; and

a first metal diffusion barrier layer formed on said first metal layer and said first insulating interlayer,

wherein said first metal diffusion barrier layer comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

Claim 217. (previously presented): A semiconductor device comprising:

an insulating underlayer;

a first insulating interlayer formed on said insulating underlayer, said first insulating interlayer having a groove;

a first metal layer having silicon atoms diffused within said first metal layer, and wherein said metal layer is buried in said groove; and a first metal diffusion barrier layer formed on said first metal layer and said first insulating interlayer,

further comprising a first etching stopper between said insulating underlayer and said first insulating interlayer.

Claim 218. (previously presented): A semiconductor device comprising:

an insulating underlayer;

a first insulating interlayer formed on said insulating underlayer, said first insulating interlayer having a groove;

a first metal layer having silicon atoms diffused within said first metal layer, and wherein said metal layer is buried in said groove; and

a first metal diffusion barrier layer formed on said first metal layer and said first insulating interlayer,

further comprising a first etching stopper between said insulating underlayer and said first insulating interlayer, wherein said first etching stopper layer is a SiCN layer.